

**CLAIMS:**

1 1. A method for utilizing bits in an illegal op code in order to not increase the  
2 number of bits required to represent each instruction comprising the steps of:

3 fetching a plurality of instructions from a memory;

4 re-encoding one or more illegal op codes of one or more instructions into a  
5 single illegal op code if said one or more instructions comprise illegal op codes that  
6 are a member of a group of illegal op codes;

7 pre-decoding a fetched instruction that does not have an illegal op code; and

8 re-encoding one or more fields of said pre-decoded instruction into a  
9 previously illegal op code which was re-mapped into said single illegal op code.

1 2. The method as recited in claim 1, wherein said pre-decoding produces  
2 additional pre-decoded information, wherein said re-encoded pre-decoded instruction  
3 is configured to store said additional pre-decoded information in said previously  
4 illegal op code.

1 3. The method as recited in claim 2, wherein said additional pre-decoded  
2 information comprises a carry-out field.

1 4. The method as recited in claim 3, wherein said carry-out field is associated  
2 with a fetched branch instruction.

1 5. A processor, comprising:  
2 an instruction cache configured to fetch a plurality of instructions; and  
3 a logic unit coupled to said instruction cache configured to re-encode one or  
4 more illegal op codes of one or more instructions into a single illegal op code if said  
5 one or more instructions comprise illegal op codes that are a member of a group of  
6 illegal op codes, wherein said logic unit is further configured to pre-decode a fetched  
7 instruction that does not have an illegal op code, wherein said logic unit is further  
8 configured to re-encode one or more fields of said pre-decoded instruction into a  
9 previously illegal op code which was re-mapped into said single illegal op code.

1 6. The processor as recited in claim 5, wherein said pre-decoding produces  
2 additional pre-decoded information, wherein said re-encoded pre-decoded instruction  
3 is configured to store said additional pre-decoded information in said previously  
4 illegal op code.

1 7. The processor as recited in claim 6, wherein said additional pre-decoded  
2 information comprises a carry-out field.

1 8. The processor as recited in claim 7, wherein said carry-out field is associated  
2 with a fetched branch instruction.

1 9. A processor, comprising:  
2 means for fetching a plurality of instructions from a memory;  
3 means for re-encoding one or more illegal op codes of one or more  
4 instructions into a single illegal op code if said one or more instructions comprise  
5 illegal op codes that are a member of a group of illegal op codes;  
6 means for pre-decoding a fetched instruction that does not have an illegal op  
7 code; and  
8 means for re-encoding one or more fields of said pre-decoded instruction into  
9 a previously illegal op code which was re-mapped into said single illegal op code.

1 10. The processor as recited in claim 9, wherein said pre-decoding produces  
2 additional pre-decoded information, wherein said re-encoded pre-decoded instruction  
3 is configured to store said additional pre-decoded information in said previously  
4 illegal op code.

1 11. The processor as recited in claim 10, wherein said additional pre-decoded  
2 information comprises a carry-out field.

1 12. The processor as recited in claim 11, wherein said carry-out field is associated  
2 with a fetched branch instruction.

1 13. A system, comprising:  
2 a memory configured to store instructions;  
3 an instruction cache coupled to said memory, wherein said instruction cache is  
4 configured to fetch a plurality of instructions from said memory; and  
5 a logic unit coupled to said instruction cache configured to re-encode one or  
6 more illegal op codes of one or more instructions into a single illegal op code if said  
7 one or more instructions comprise illegal op codes that are a member of a group of  
8 illegal op codes, wherein said logic unit is further configured to pre-decode a fetched  
9 instruction that does not have an illegal op code, wherein said logic unit is further  
10 configured to re-encode one or more fields of said pre-decoded instruction into a  
11 previously illegal op code which was re-mapped into said single illegal op code.

1 14. The system as recited in claim 13, wherein said pre-decoding produces  
2 additional pre-decoded information, wherein said re-encoded pre-decoded instruction  
3 is configured to store said additional pre-decoded information in said previously  
4 illegal op code.

1 15. The system as recited in claim 14, wherein said additional pre-decoded  
2 information comprises a carry-out field.

1 16. The system as recited in claim 15, wherein said carry-out field is associated  
2 with a fetched branch instruction.